IN THE CLAIMS

Please amend claims 1-3, 6, 7, 21, 23, 25, 26, 27, 30, 45, 47, 49-51, 54, 73, 74, and 76 as follows:

1. (Currently Amended) An input port to a switching core, comprising:

a) an input policing unit that checks if a virtual lane has a sufficient number of credits to carry an input packet being received by said input policing unit;

b) a request manager that generates a request for said packet to be switched by said switching core;

c) a packet Rx unit that stores said packet into a memory by writing blocks of data into said memory;

d) a packet Tx unit that receives a grant in response to said request and reads said packet from said memory in response to said grant by reading said blocks of data, wherein said grant may be received by said packet Tx unit before said packet is completely stored in said memory; and

e) a pointer RAM manager that provides addresses of free blocks of data within said memory to said packet Rx unit and receives addresses of freed blocks of data within said memory from said packet Tx unit.

2. (Currently Amended) The input port of claim 1 wherein, if said packet is a ~~VL15~~ packet that flows upon a virtual lane reserved for network information, said input policing unit does not check if a virtual lane has a sufficient number of credits.

3. (Currently Amended) The input port of claim 1 wherein said request further comprises information from said packet's header, said information comprising:

1) a size of said packet;

2) whether or not said packet is a ~~VL15~~ packet that flows upon a virtual lane reserved for network information;

3) a service level (SL) of said packet;

4) a destination address of said packet; and

5) a pointer that corresponds to an address for a first block of said blocks.

4. (Previously Presented) The input port of claim 3 wherein said information further comprises which partition said packet belongs to if said packet belongs to a partition.

5. (Previously Presented) The input port of claim 1 wherein said request can be generated by said request manager before said packet is completely stored into said memory.

6. (Currently Amended) The input port of claim 5 wherein said request manager:

1) generates said request in response to said packet being recognized as a ~~VL15~~ packet that flows upon a virtual lane reserved for network information, or, if said packet is not recognized as ~~VL15~~ a packet that flows upon a virtual lane reserved for network information~~:~~;

2) generates said request in response to identifying a partition to which said packet belongs to if said request manager is told to check for partition information, or, if said request manager is not told to check for partition information~~:~~;

3) generates said request in response to identifying a size of said packet.

7. (Currently Amended) The input port of claim 5 wherein if said grant ~~may be~~is received by said packet Tx unit before said packet is completely stored into said memory ~~and, as a consequence~~, said packet Tx unit will begin to said read said packet from said memory before said packet is completely stored into said memory.

8. (Previously Presented) The input port of claim 1 wherein said packet Rx unit asks said request manager for one address for a free block within said memory for each one of said blocks of data that are written into said memory.

9. (Previously Presented) The input port of claim 8 wherein said memory further comprises a plurality of individual random access memories (RAMs), said packet Rx unit configured to utilize a block of data's corresponding address for a free block at each of said individual RAMs while writing said block into said memory.

10. (Previously Presented) The input port of claim 9 wherein said packet Rx unit is configured to increment said corresponding address to produce a second address that is utilized at each of said individual RAMs while writing said block into said memory.

11. (Previously Presented) The input port of claim 10 wherein said packet Rx unit is configured to increment said second address to produce a third address that is utilized at each of said individual RAMs while writing said block into said memory.

12. (Previously Presented) The input port of claim 11 wherein said packet Rx unit is configured to increment said third address to produce a fourth address that is utilized at each of said individual RAMs while writing said block into said memory.

13. (Previously Presented) The input port of claim 12 wherein said plurality of individual RAMs further comprises four individual RAMs.

14. (Previously Presented) The input port of claim 8 wherein said input port further comprises an Error RAM, said packet Rx unit configured to write to said Error RAM, for each block of data that is written into said memory, to indicate whether said block of data has an error.

15. (Previously Presented) The input port of claim 8 wherein said input port further comprises a Virtual Lane RAM, said packet configured to write to said Virtual Lane RAM, for each block of data from said packet that is written into said memory, to indicate said virtual lane that said packet traveled across.

16. (Previously Presented) The input port of claim 1 wherein said input port further comprises a Pointer RAM, said Pointer RAM to store a link list of those address of said memory used to store said packet within said memory, said Pointer RAM also to store a link list of those addresses of said memory that are free blocks of data within said memory, both of said link lists maintained by said pointer RAM manager.

17. (Previously Presented) The input port of claim 1 wherein said memory further comprises a plurality of individual random access memories (RAMs) and said packet Tx unit further comprises a plurality of read channels, each one of said read channels to read from a different one of said memories, said plurality of read channels arranged in a serial loop with a control unit, said control unit to enter a read address into said loop so that a series of reads are made from each of said read channel units at said read address and to remove said read address from said loop after each of said read channels have performed their read with said read address.

18. (Previously Presented) The input port of claim 17 wherein said control loop receives, from said pointer manager, one read address to be entered into within said loop for each one of said blocks of data that are read from said memory.

19. (Previously Presented) The input port of claim 17 wherein said control unit can enter into said loop a second read address where data from a second packet is stored within said memory, said second read address within said loop while said read address is also within said loop so that data from said packet can be read from said memory via a first of said read channels while data from said second packet is being read from said memory via a second of said read channels.

20. (Previously Presented) The input port of claim 19 wherein said packet Tx unit further comprises four read channels and said control unit can enter up to three different read address within said loop so that data from three different packets can be simultaneously read from said memory.

21. (Currently Amended) The input port of claim 17 wherein said packet Tx unit further comprises a multiplexer, said multiplexer having an output that provides said packet to said switching core, said multiplexer having a different input for each of said read channels, each read channel output coupled to a different one of said multiplexer inputs, said multiplexer provided a series of channel select values over time that cause said multiplexer to select the

output of whichever read channel has said read address so as to synchronize said ~~mutliplexer's~~multiplexer's input selection with said read address's travels through said loop.

22. (Previously Presented) The input port of claim 21 wherein said control unit can enter into said loop a second read address where data from a second packet is stored within said memory, said second read address within said loop while said read address is also within said loop so that data from said packet can be read from said memory via a first of said read channels while data from said second packet is being read from said memory via a second of said read channels.

23. (Currently Amended) The input port of claim 22 wherein said packet Tx unit further comprises a second multiplexer, said second multiplexer having an output that provides said second packet to said switching core, said second multiplexer having a different input for each of said read channels, each read channel output coupled to a different one of said second multiplexer inputs, said second multiplexer provided a series of channel select value over time that cause said second multiplexer to select the output of whichever read channel has said second read address so as to synchronize said second ~~mutliplexer's~~multiplexer's input selection with said second read address's travels through said loop.

24. (Previously Presented) The input port of claim 1 wherein, if said packet is to be multicasted, a unique grant is received by said packet Tx unit for each copy of said packet to be sent to said switching core, each unique grant having a first number, said first number indicating how many copies of said packet are to be sent to said switching core in order to fulfill said multicasting effort, said packet Tx unit coupled to a Grant RAM, said Grant RAM to maintain a second number that reflects how many copies of said packet have been sent to said switching core, said packet Tx unit configured to increment said second number if, after said increment, said second number is less than said first number.

25. (Currently Amended) A switch, comprising:

a) a switching core that switches a packet;

b) an arbiter that receives a request to switch said packet through said switch;

c) an input port that receives said packet, said input port coupled to both said switching core and said arbiter, said input port further comprising:

1) a request manager that generates said request;

2) a packet Rx unit that stores said packet into a memory by writing blocks of data into said memory;

3) a packet Tx unit that receives a grant from said arbiter in response to said request and reads said packet from said memory in response to said grant by reading said blocks of data; and

4) a pointer RAM manager that provides addresses for free blocks of data within said memory to said packet Rx unit and receives addresses of freed blocks of data within said memory from said packet Tx unit; and

d) an output port that receives said packet from said switching core.

26. (Currently Amended) The input port of claim 25 wherein, if said packet is a ~~VL15~~ packet that flows upon a virtual lane reserved for network information, an input policing unit within said input port does not check if a virtual lane has a sufficient number of credits.

27. (Currently Amended) The input port of claim 25 wherein said request further comprises information from said packet's header, said information comprising:

1) a size of said packet;

2) whether or not said packet is a ~~VL15~~ packet that flows upon a virtual lane reserved for network information;

3) a service level (SL) of said packet;

4) a destination address of said packet; and

5) a pointer that corresponds to an address for a first block of said blocks.

28. (Previously Presented) The input port of claim 27 wherein said information further comprises which partition said packet belongs to if said packet belongs to a partition.

29. (Previously Presented) The input port of claim 25 wherein said request can be generated by said request manager before said packet is completely stored into said memory.

30. (Currently Amended) The input port of claim 29 wherein said request manager:

1) generates said request in response to said packet being recognized as a ~~VL15~~ packet that flows upon a virtual lane reserved for network information, or, if said packet is not recognized as a ~~VL15~~ packet that flows upon a virtual lane reserved for network information~~:~~;

2) generates said request in response to identifying a partition to which said packet belongs to if said request manager is told to check for partition information, or, if said request manager is not told to check for partition information~~:~~;

3) generates said request in response to identifying a size of said packet.

31. (Previously Presented) The input port of claim 29 wherein said grant may be received by said packet Tx unit before said packet is completely stored into said memory and, as a consequence, said packet Tx unit will begin to said read said packet from said memory before said packet is completely stored into said memory.

32. (Previously Presented) The input port of claim 25 wherein said packet Rx unit asks said request manager for one address for a free block within said memory for each one of said blocks of data that are written into said memory.

33. (Previously Presented) The input port of claim 32 wherein said memory further comprises a plurality of individual random access memories (RAMs), said packet Rx unit configured to utilize a block of data's corresponding address for a free block at each of said individual RAMs while writing said block into said memory.

34. (Previously Presented) The input port of claim 33 wherein said packet Rx unit is configured to increment said corresponding address to produce a second address that is utilized at each of said individual RAMs while writing said block into said memory.

35. (Previously Presented) The input port of claim 34 wherein said packet Rx unit is configured to increment said second address to produce a third address that is utilized at each of said individual RAMs while writing said block into said memory.

36. (Previously Presented) The input port of claim 35 wherein said packet Rx unit is configured to increment said third address to produce a fourth address that is utilized at each of said individual RAMs while writing said block into said memory.

37. (Previously Presented) The input port of claim 36 wherein said plurality of individual RAMs further comprises four individual RAMs.

38. (Previously Presented) The input port of claim 32 wherein said input port further comprises an Error RAM, said packet Rx unit configured to write to said Error RAM, for each block of data that is written into said memory, to indicate whether said block of data has an error.

39. (Previously Presented) The input port of claim 32 wherein said input port further comprises a Virtual Lane RAM, said packet configured to write to said Virtual Lane RAM, for each block of data from said packet that is written into said memory, to indicate said virtual lane that said packet traveled across.

40. (Previously Presented) The input port of claim 25 wherein said input port further comprises a Pointer RAM, said Pointer RAM to store a link list of those address of said memory used to store said packet within said memory, said Pointer RAM also to store a link list of those addresses of said memory that are free blocks of data within said memory, both of said link lists maintained by said pointer RAM manager.

41. (Previously Presented) The input port of claim 25 wherein said memory further comprises a plurality of individual random access memories (RAMs) and said packet Tx unit further comprises a plurality of read channels, each one of said read channels to read from a different one of said memories, said plurality of read channels arranged in a serial loop with a

control unit, said control unit to enter a read address into said loop so that a series of reads are made from each of said read channel units at said read address and to remove said read address from said loop after each of said read channels have performed their read with said read address.

42. (Previously Presented) The input port of claim 41 wherein said control loop receives, from said pointer manager, one read address to be entered into within said loop for each one of said blocks of data that are read from said memory.

43. (Previously Presented) The input port of claim 41 wherein said control unit can enter into said loop a second read address where data from a second packet is stored within said memory, said second read address within said loop while said read address is also within said loop so that data from said packet can be read from said memory via a first of said read channels while data from said second packet is being read from said memory via a second of said read channels.

44. (Previously Presented) The input port of claim 43 wherein said packet Tx unit further comprises four read channels and said control unit can enter up to three different read address within said loop so that data from three different packets can be simultaneously read from said memory.

45. (Currently Amended) The input port of claim 41 wherein said packet Tx unit further comprises a multiplexer, said multiplexer having an output that provides said packet to said switching core, said multiplexer having a different input for each of said read channels, each read channel output coupled to a different one of said multiplexer inputs, said multiplexer provided a series of channel select values over time that cause said multiplexer to select the output of whichever read channel has said read address so as to synchronize said ~~mutliplexer's~~multiplexer's input selection with said read address's travels through said loop.

46. (Previously Presented) The input port of claim 45 wherein said control unit can enter into said loop a second read address where data from a second packet is stored within said

memory, said second read address within said loop while said read address is also within said loop so that data from said packet can be read from said memory via a first of said read channels while data from said second packet is being read from said memory via a second of said read channels.

47. (Currently Amended) The input port of claim 46 wherein said packet Tx unit further comprises a second multiplexer, said second multiplexer having an output that provides said second packet to said switching core, said second multiplexer having a different input for each of said read channels, each read channel output coupled to a different one of said second multiplexer inputs, said second multiplexer provided a series of channel select values over time that cause said second multiplexer to select the output of whichever read channel has said second read address so as to synchronize said second ~~mutliplexer's~~multiplexer's input selection with said second read address's travels through said loop.

48. (Previously Presented) The input port of claim 25 wherein, if said packet is to be multicasted, a unique grant is received by said packet Tx unit for each copy of said packet to be sent to said switching core, each unique grant having a first number, said first number indicating how many copies of said packet are to be sent to said switching core in order to fulfill said multicasting effort, said packet Tx unit coupled to a Grant RAM, said Grant RAM to maintain a second number that reflects how many copies of said packet have been sent to said switching core, said packet Tx unit configured to increment said second number if, after said increment, said second number is less than said first number.

49. (Currently Amended) A method, comprising:

checking if a virtual lane has a sufficient number of credits to carry a packet that is being received;

generating a request for said packet to be switched by a switching core;

storing said packet into a memory by writing blocks of data into said memory, said writing making use of addresses for free blocks of data within said memory;

receiving a grant in response to said request; and

reading said packet from said memory, in response to said grant, by reading said blocks of data, said writing freeing blocks of data within said memory, wherein said grant may be received before said packet is completely stored in said memory.

50. (Currently Amended) The method of claim 48 wherein, if said packet is a ~~VL15~~ packet that flows upon a virtual lane reserved for network information, checking if a virtual lane has a sufficient number of credits is not performed.

51. (Currently Amended) The method of claim 48 wherein said request further comprises information from said packet's header, said information comprising:

1) a size of said packet;

2) whether or not said packet is a ~~VL15~~ packet that flows upon a virtual lane reserved for network information;

3) a service level (SL) of said packet;

4) a destination address of said packet; and

5) a pointer that corresponds to an address for a first block of said blocks.

52. (Previously Presented) The method of claim 51 wherein said information further comprises which partition said packet belongs to if said packet belongs to a partition.

53. (Previously Presented) The method of claim 49 further comprising generating said request before said request is completely stored into said memory.

54. (Currently Amended) The method of claim 53 further comprising:

1) generating said request in response to said packet being recognized as a ~~VL15~~ packet that flows upon a virtual lane reserved for network information, or, if said packet is not recognized as ~~VL15~~ a packet that flows upon a virtual lane reserved for network information~~:~~;

2) generating said request in response to identifying a partition to which said packet belongs to if a partition checking feature is activated, or, if said partition checking feature is not activated~~:~~;

3) generating said request in response to identifying a size of said packet.

55. (Previously Presented) The method of claim 54 further comprising receiving said grant before said packet is completely stored into said memory and, as a consequence, beginning to said read said packet from said memory before said packet is completely stored into said memory.

56. (Previously Presented) The method of claim 49 further comprising asking for one address for a free block within said memory for each one of said blocks of data that are written into said memory.

57. (Previously Presented) The method of claim 56 wherein said memory further comprises a plurality of individual random access memories (RAMs), said method further comprising utilizing a block of data's corresponding address for a free block at each of said individual RAMs while writing said block into said memory.

58. (Previously Presented) The method of claim 57 further comprising incrementing said corresponding address to produce a second address that is utilized at each of said individual RAMs while writing said block into said memory.

59. (Previously Presented) The method of claim 58 further comprising incrementing said second address to produce a third address that is utilized at each of said individual RAMs while writing said block into said memory.

60. (Previously Presented) The method of claim 59 further comprising incrementing said third address to produce a fourth address that is utilized at each of said individual RAMs while writing said block into said memory.

61. (Previously Presented) The method of claim 60 wherein said plurality of individual RAMs further comprises four individual RAMs.

62. (Previously Presented) The method of claim 56 further comprising writing to an Error RAM, for each block of data that is written into said memory, to indicate whether said block of data has an error.

63. (Previously Presented) The method of claim 56 further comprising writing to a Virtual Lane RAM, for each block of data from said packet that is written into said memory, to indicate said virtual lane that said packet traveled across.

64. (Previously Presented) The method of claim 49 further comprising generating a link list of those addresses of said memory used to store said packet within said memory.

65. (Previously Presented) The method of claim 49 wherein said memory further comprises a plurality of individual random access memories (RAMs) said reading further comprising circulating a read address through a series of read channels, each one of said read channels to read from a different one of said memories, so that a series of reads are made from each of said read channel units at said read address.

66. (Previously Presented) The method of claim 65 further comprising entering one requested read address into a loop that is at least partially formed by said series of read channels for each one of said blocks of data that are read from said memory.

67. (Previously Presented) The method of claim 65 further comprising circulating a second read address where data from a second packet is stored within said memory, said second read address being circulated while said read address is being circulated so that data from said packet can be read from said memory via a first of said read channels while data from said second packet is being read from said memory via a second of said read channels.

68. (Previously Presented) The method of claim 67 further comprising circulating three different read addresses so that data from three different packets can be simultaneously read from said memory.

69. (Previously Presented) The method of claim 65 further comprising multiplexing each read channel output to a first input of said switching core while said read address is said circulating so that said packet is sent to said switching core through said first input.

70. (Previously Presented) The method of claim 69 further comprising circulating a second read address where data from a second packet is stored within said memory, said second read address being circulated while said read address is being circulated so that data from said packet can be read from said memory via a first of said read channels while data from said second packet is being read from said memory via a second of said read channels.

71. (Previously Presented) The method of claim 70 further comprising multiplexing each read channel output to a second input of said switching core while said second read address is said circulating so that said second packet is sent to said switching core through said second input.

72. (Previously Presented) The method of claim 49 wherein, if said packet is to be multicasted, a unique grant is received for each copy of said packet to be sent to said switching core, each unique grant having a first number, said first number indicating how many copies of said packet are to be sent to said switching core in order to fulfill said multicasting effort, said method further comprising maintaining a second number that reflects how many copies of said packet have been sent to said switching core, said method further comprising incrementing said second number if, after said increment, said second number is less than said first number.

73. (Currently Amended) An apparatus, comprising:

means for checking if a virtual lane has a sufficient number of credits to carry a packet that is being received;

means for generating a request for said packet to be switched by a switching core;

means for storing said packet into a memory by writing blocks of data into said memory, said writing making use of addresses for free blocks of data within said memory;

means for receiving a grant in response to said request; and

means for reading said packet from said memory, in response to said grant, by reading said blocks of data, said writing freeing blocks of data within said memory, wherein said grant may be received before said packet is completely stored in said memory.

74. (Currently Amended) The apparatus of claim 73 wherein said request further comprises information from said packet's header, said information comprising:

1) a size of said packet;

2) whether or not said packet is a ~~VL15~~ packet that flows upon a virtual lane reserved for network information;

3) a service level (SL) of said packet;

4) a destination address of said packet; and

5) a pointer that corresponds to an address for a first block of said blocks.

75. (Previously Presented) The apparatus of claim 73 further comprising means for generating said request before said request is completely stored into said memory.

76. (Currently Amended) The apparatus of claim 75 wherein said means for generating said request before said request is completely stored into said memory further comprises means for:

1) generating said request in response to said packet being recognized as a ~~VL15~~ packet that flows upon a virtual lane reserved for network information, or, if said packet is not recognized as a ~~VL15~~ packet that flows upon a virtual lane reserved for network information~~:~~;

2) generating said request in response to identifying a partition to which said packet belongs to if a partition checking feature is activated, or, if said partition checking feature is not activated~~:~~;

3) generating said request in response to identifying a size of said packet.

77. (Previously Presented) The apparatus of claim 74 further comprising means for receiving said grant before said packet is completely stored into said memory and means for

beginning to said read said packet from said memory before said packet is completely stored into said memory as a consequence.

78. (Previously Presented) The apparatus of claim 73 further comprising means for asking for one address for a free block within said memory for each one of said blocks of data that are written into said memory.

79. (Previously Presented) The apparatus of claim 78 wherein said memory further comprises a plurality of individual random access memories (RAMs), said apparatus further comprising means for utilizing a block of data's corresponding address for a free block at each of said individual RAMs while writing said block into said memory.

80. (Previously Presented) The apparatus of claim 73 further comprising generating a link list of those addresses of said memory used to store said packet within said memory.

81. (Previously Presented) The apparatus of claim 73 wherein said memory further comprises a plurality of individual random access memories (RAMs), said means for reading further comprising means for circulating a read address through a series of read channels, each one of said read channels to read from a different one of said memories, so that a series of reads are made from each of said read channel units at said read address.